REMARKS

The present amendment is in response to the Office Action dated October 25, 2002, where the Examiner has rejected claims 1-18. By the present amendment and response, claim 10 and Figure 11 have been amended to overcome the Examiner's objections. Reconsideration and allowance of pending claims 1-18 in view of the following remarks are respectfully requested.

A. Objection to Drawings

The Examiner has objected to the drawings as failing to comply with 37 CFR §1.84(p)(5). In particular, the Examiner states that Figure 11 includes reference numeral "1100" and the specification does not disclose reference numeral "1100." To overcome the objection, Applicants have amended Figure 11 to delete reference numeral "1100." Accordingly, Applicants respectfully submit that the objection to the drawings has been traversed.

The Examiner has objected to the drawings under 37 CFR §1.83(a). In particular, and with reference to claim 10, the Examiner has stated that the drawings must show every feature of the invention specified in that claim. Applicants submit that amended claim 10 overcomes the Examiner's objection under 37 CFR §1.83(a).

B. Rejection of Claim 10 under 35 U.S.C. § 112

The Examiner has rejected claim 10 under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification. Applicants

submit that amended claim 10 overcomes the Examiner's rejection under 35 USC §112, first paragraph.

C. **Rejection of Claims 10 and 16 under 35 U.S.C. § 102**

The Examiner has rejected claims 10 and 16 under 35 USC §102 as being anticipated by **Tsunemitsu et al.** (USPN 3,862,017) ("**Tsunemitsu '017**"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claim 10, is patentably distinguishable over **Tsunemitsu '017**.

Pending claims 10 and 16 are directed to a metal resistor in an IC chip. The present invention, as recited in amended independent claim 10, teaches a chip including, among other things, "a first interconnect metal layer; a first intermetallic dielectric layer situated over said first interconnect metal layer; a metal resistor situated over said first intermetallic dielectric layer and below a second intermetallic dielectric layer; a second interconnect metal layer over said second intermetallic dielectric layer; a first intermediate via connected to a first terminal of said metal resistor; [and] a second intermediate via connected to a second terminal of said metal resistor."

In contrast, **Tsunemitsu '017** does not teach, disclose, or suggest a chip that includes the above recited limitations specified by claim 10. **Tsunemitsu '017** discloses a method for producing a thin film passive circuit element. In particular, **Tsunemitsu '017** teaches semiconductor device 20 including resistor 16 connected to aluminum wiring path 14 and aluminum wiring path 28. Aluminum wiring path 14 is situated in a lower metal layer than aluminum wiring path 28. Resistor 16 is connected to aluminum

wiring path 28 by a single connection. For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by independent claim 10, is not suggested, disclosed, or taught by **Tsunemitsu '017**. As such, the present invention, as defined by independent claim 10, is patentably distinguishable over **Tsunemitsu '017** and claim 16 depending from independent claim 10 is, *a fortiori*, also patentably distinguishable over **Tsunemitsu '017**.

D. Rejection of Claims 1-9, 11-15 and 17-18 under 35 U.S.C. § 103

The Examiner has rejected claims 1 and 3 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017** in view of **Nalin Kumar** (USPN 5,120,572) ("**Kumar '572**"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claim 1, is patentably distinguishable over **Tsunemitsu '017**, **Kumar '572** or any combination thereof.

Pending claims 1 and 3 are directed to directed to a metal resistor in an IC chip. The present invention, as recited in independent claim 1, teaches a chip including, among other things, "a first intermediate via connected to a first terminal of said metal resistor, said first intermediate via being further connected to a first metal segment patterned in said second interconnect metal layer; a second intermediate via connected to a second terminal of said metal resistor, said second intermediate via being further connected to a second metal segment patterned in said second interconnect metal layer."

In contrast, **Tsunemitsu '017** and **Kumar '572** do not, singly or in combination teach, disclose, or suggest a chip that includes the above recited limitations specified by

claim 1. As discussed above, **Tsunemitsu '017** discloses a method for producing a thin film passive circuit element. **Tsunemitsu '017** does not teach, disclose, or suggest a chip that includes, among other things, "a first intermediate via connected to a first terminal of said metal resistor, said first intermediate via being further connected to a first metal segment patterned in said second interconnect metal layer; a second intermediate via connected to a second terminal of said metal resistor, said second intermediate via being further connected to a second metal segment patterned in said second interconnect metal layer." Moreover, **Tsunemitsu '017** teaches away from the present invention, as recited in claim 1, because **Tsunemitsu '017** teaches connecting a resistor to a metal layer that is closer to the substrate, which increases parasitic capacitance.

Kumar '572 discloses a method of fabricating electrical components in high density substrates. In particular, **Kumar '572** discloses an integrated resistor including resistor 48, substrate 40, via 84 and electrical connections 92 and 94. Resistor 48 is situated over, and in direct contact with, substrate 40. Electrical connections 92 and 94 are situated above, and electrically connected to, resistor 48 by via 84. Thus, **Kumar '572** does not teach, disclose, or suggest a chip that includes, among other things, "a first interconnect metal layer; a first intermetallic dielectric layer situated over said first interconnect metal layer; a metal resistor situated over said first intermetallic dielectric layer and below a second intermetallic dielectric layer; a second interconnect metal layer over said second intermetallic dielectric layer." In particular, **Kumar '572** does not teach, disclose, or suggest a metal resistor situated between a first interconnect metal

layer and a second interconnect metal layer because **Kumar '572** only teaches a resistor 48 situated beneath electrical connections 92 and 94. Moreover, **Kumar '572** teaches away from the present invention, as recited in claim 1, because **Kumar '572** does not teach a metal resistor situated over a first intermetallic dielectric layer. In contrast, **Kumar '572** teaches a resistor situated over, and in direct contact with, the substrate, which increases parasitic capacitance.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by **Tsunemitsu '017**, **Kumar '572** or any combination thereof. As such, the present invention, as defined by independent claim 1, is patentably distinguishable over **Tsunemitsu '017** and **Kumar '572**. Further, claim 3 depending from independent claim 1 is, *a fortiori*, also patentably distinguishable over **Tsunemitsu '017** and **Kumar '572**.

Applicants respectfully submit that there is no teaching or suggestion to combine **Tsunemitsu '017** or **Kumar '572** to obtain an integrated circuit chip recited in independent claim 1. Thus, independent claim 1 and dependent claim 3 are patentably distinguishable over **Tsunemitsu '017**, **Kumar '572** or any combination thereof.

The Examiner has further rejected claim 2 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017** and **Kumar '572** as applied to claim 1, and further in view of **Kato et al.** (USPN 4,795,921) ("**Kato '921**"). As discussed above, independent claim 1 is patentably distinguishable over **Tsunemitsu '017** and **Kumar '572** and, as

such, claim 2 depending from independent claim 1 is, *a fortiori*, patentable over the cited references.

The Examiner has further rejected claims 4 and 5 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017** in view of **Kumar '572**. As discussed above, independent claim 1 is patentably distinguishable over **Tsunemitsu '017** and **Kumar '572** and, as such, claims 4 and 5 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over **Tsunemitsu '017** and **Kumar '572**.

The Examiner has further rejected claims 6 and 7 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017** and **Kumar '572** as applied to claim 1, and in further view of **Yuang et al.** (USPN 6,232,194) ("**Yuang '194**"). As discussed above, independent claim 1 is patentably distinguishable over **Tsunemitsu '017** and **Kumar '572** and, as such, claims 6 and 7 depending from independent claim 1 are, *a fortiori*, patentable over the cited references.

The Examiner has further rejected claims 8 and 9 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017** and **Kumar '572** as applied to claim 1, and in further view of **Ohkawa et al.** (USPN 5,525,831) ("**Ohkawa '831**"). As discussed above, independent claim 1 is patentably distinguishable over **Tsunemitsu '017** and **Kumar '572** and, as such, claims 8 and 9 depending from independent claim 1 are, *a fortiori*, patentable over the cited references.

The Examiner has further rejected claim 11 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017** in view of **Kato '921**. As discussed above, the present invention, as defined by independent claim 10, is patentably distinguishable over **Tsunemitsu '017** and, as such, claim 11 depending from independent claim 10 is, *a fortiori*, also patentable over the cited references.

The Examiner has further rejected claims 12 and 13 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017**. As discussed above, independent claim 10 is patentably distinguishable over **Tsunemitsu '017** and, as such, claims 12 and 13 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over **Tsunemitsu '017**.

The Examiner has further rejected claims 14 and 15 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017** in view of **Yuang '194**. As discussed above, independent claim 10 is patentably distinguishable over **Tsunemitsu '017** and, as such, claims 14 and 15 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over the cited references.

The Examiner has further rejected claims 17 and 18 under 35 USC §103(a) as being unpatentable over **Tsunemitsu '017** in view of **Ohkawa '831**. As discussed above, independent claim 10 is patentably distinguishable over **Tsunemitsu '017** and, as such, claims 17 and 18 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over the cited references.

E. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 10, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-18 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-18 pending in the present application is respectfully requested.

Respectfully Submitted,
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Date: 2/14/03

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 10 has been amended as follows:

10. (Once Amended) An integrated circuit chip comprising:

a first interconnect metal layer;

a first intermetallic dielectric layer situated over said first interconnect metal layer;

a metal resistor situated over said first intermetallic dielectric layer and below a second intermetallic dielectric layer;

a second interconnect metal layer over said second intermetallic dielectric layer;

a first intermediate via connected to a first terminal of said metal resistor[, said first intermediate via being further connected to a first metal segment patterned in said first interconnect metal layer];

a second intermediate via connected to a second terminal of said metal resistor[, said second intermediate via being further connected to a second metal segment patterned in said first interconnect metal layer].

In the Drawings:

Reference numeral 1100 has been removed from Figure 11. A clean copy of Figure 11 is attached.